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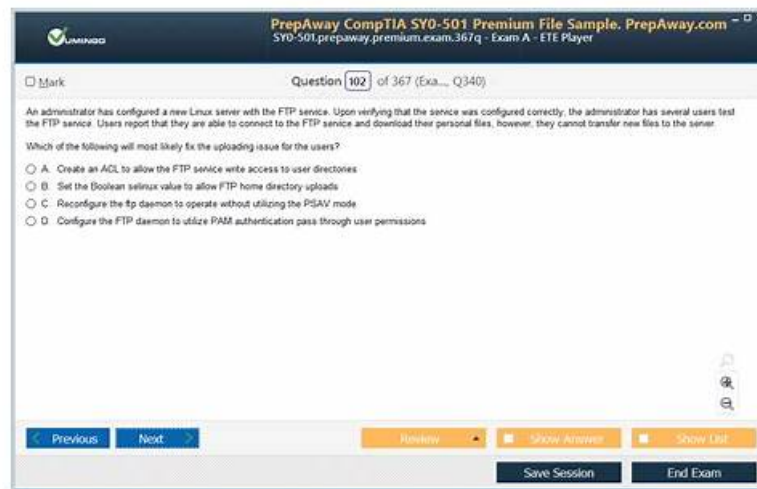
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Pure Storage Certified FlashArray Implementation Specialist Sample Questions (Q50-Q55):

NEW QUESTION # 50
What upgrade scenario required an upgrade of power supplies?

- A. X50 > X70
- B. X10 > X50
- C. X50R2 > X50R3

Answer: B

Explanation:
The upgrade from a FlashArray//X10 (or X20) to a FlashArray//X50 requires a mandatory power supply unit (PSU) upgrade.
While the FlashArray//X series utilizes a shared chassis design (3U) for models X10 through X90, the power requirements differ
significantly between the entry-level and performance-tier controllers.
X10/X20: These models typically ship with 1000W or 1200W power supplies, which are sufficient for their lower-power CPUs and
component loads.
X50/X70/X90: These "Performance" class arrays utilize higher-wattage Intel Xeon processors and often support denser NVMe
configurations, necessitating 1600W power supplies to ensure stability and N+1 redundancy.
When a customer performs a Data-in-Place upgrade (swapping controllers) from an X10 to an X50, the existing chassis is retained,
but the lower-capacity PSUs must be physically swapped for the high-capacity 1600W units to support the new X50 controllers.
Conversely, upgrades like X50 > X70 (Option B) or R2 > R3 (Option C) typically occur within the same power tier, utilizing the
existing 1600W PSUs.

NEW QUESTION # 51
Which Purity command can be used to validate I/O is balanced across initiators?

- A. purehost iobalance --check
- B. purehost list --balance
- C. purehost monitor --balance

Answer: C

Explanation:
To validate that I/O traffic is correctly distributed across a host's initiators (Fibre Channel WWNs or iSCSI IQNs), the correct
command is purehost monitor --balance.
Ensuring "multipathing balance" is a critical post-installation check. If a host is configured correctly with Multipath I/O (MPIO)
software (like DM-Multipath on Linux or MPIO on Windows), read/write requests should be distributed relatively evenly across all
active paths to the storage array.
Command Function: The purehost monitor command provides real-time performance statistics for hosts. Adding the --balance flag
switches the view to a granular breakdown of IOPS and Bandwidth per initiator for the specified host.
Interpretation: An Implementation Engineer looks for initiators showing 0 IOPS or significantly lower traffic than others, which would
indicate a path failure, zoning issue, or incorrect MPIO policy (e.g., Failover Only instead of Round Robin). Options A and B are
incorrect syntax; purehost list shows configuration (not real-time stats), and iobalance is not a valid Purity command argument.

NEW QUESTION # 52
Which NVRAM bays are always populated on the FlashArray//XR2/3?

- A. 0-1
- B. 0-3
- C. 0-2

Answer: A

Explanation:
The FlashArray//XR2 and //XR3 architectures utilize dedicated NVRAM modules to provide the non-volatile write cache necessary
for acknowledging writes safely before they are destaged to flash. These chassis are equipped with multiple NVRAM bays (labeled
NVB0 through NVB3).
For standard configurations, specifically the //X10, //X20, and //X50 models, the system requires a redundant pair of NVRAM
modules to function. These are always installed in NVRAM bays 0 and 1.
Bays 0 and 1 form the primary high-availability pair. If one fails, the other retains the data, and the system can continue to operate
(though often in write-through mode or with alerts).
Higher-end models like the //X70 and //X90 populate all four bays (0-3) to provide the larger write buffer required for their higher
throughput capabilities.
However, since the question asks which bays are always populated (i.e., the minimum requirement for the platform to function
across the board), the answer is the foundational pair in slots 0 and 1. An Implementation Engineer must ensure these specific slots
are populated first during any chassis maintenance or upgrade.
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NEW QUESTION # 53

An Implementation Engineer is deploying a FlashArray//XLR5 with two DirectFlash Shelves. The engineer wants to ensure the shelves are installed in the preferred PCIe slots to achieve optimal performance and support. Which PCIe slots should the Implementation Engineer use for connecting the DFS shelves?

- A. PCIe slot 1 for SH9, PCIe slot 7 for SH8
- B. PCIe slot 0 for SH9, PCIe slot 6 for SH8
- C. PCIe slot 0 for SH8, PCIe slot 8 for SH9

Answer: B

Explanation:
The FlashArray//XL platform features a split-chassis design with a unique PCIe bus layout compared to the standard //X series. To maintain optimal performance and redundancy, the backend connectivity for DirectFlash Shelves (DFS) must be balanced across the specific PCIe root complexes managed by the dual CPUs.
For a configuration involving multiple shelves (specifically targeting the logical shelf identifiers SH8 and SH9, which often correspond to the first pair of backend loops in an //XL deployment), the validated configuration is to use PCIe Slot 0 and PCIe Slot 6. These slots are architecturally designated for the backend NVMe-oF (RoCE) fabric cards.
Using Slot 0 (typically located on the far left) and Slot 6 (located on the right side of the chassis) ensures that the I/O load is distributed across the internal midplane and CPUs correctly. Placing cards in incorrect slots (like Slot 1 or 7, which might be reserved for host I/O or inter-controller links) can result in shelf detection failures or performance bottlenecks where one CPU is overloaded with backend traffic while the other is idle.
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NEW QUESTION # 54

A customer would like to reduce SafeMode settings for retention and eradication with their current policy. How is authorization obtained to make the requested changes?

- A. Two SafeMode approvers need to acknowledge via Pure1 step-up authentication before any changes can be made.
- B. A Pure1 Admin needs to approve any changes for Pure Support to proceed.
- C. The local account on FlashArray needs to permit any local changes.

Answer: A

Explanation:
To reduce SafeMode protections (such as shortening the retention period or disabling the eradication timer), two authorized SafeMode approvers must authenticate and approve the request via Pure1 step-up authentication.
SafeMode is a ransomware protection feature designed to prevent the accidental or malicious deletion of snapshots. Because reducing these protections weakens the array's security posture, Pure Storage enforces a strict "Ratchet" authorization process.
The Process: Unlike standard support requests, a single admin or local user cannot authorize this change (making Option C incorrect). The customer must have previously designated specific individuals as "SafeMode Approvers" in their Pure1 portal.
Authorization: When a request to weaken the policy is made, Pure Support triggers a verification workflow. Two of these designated approvers must log into Pure1 and perform a secondary authentication (often involving a PIN or TOTP) to explicitly "sign off" on the reduction. This "two-person rule" ensures that a compromised credential or a rogue insider cannot unilaterally expose the organization's backup data to destruction.

NEW QUESTION # 55

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