

# FlashArray-Implementation-Specialist Practice Test - FlashArray-Implementation-Specialist Training Torrent: Pure Storage Certified FlashArray Implementation Specialist - FlashArray-Implementation-Specialist Study Guide



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## Pure Storage Certified FlashArray Implementation Specialist Sample Questions (Q143-Q148):

### NEW QUESTION # 143

An Implementation Engineer is installing the first DirectFlash Shelf (DFS) on a FlashArray//XR4 controller. Which ports should the Implementation Engineer use for the connection?

- A. ETH 18/19
- B. ETH 0/1
- C. ETH 10/11

**Answer: A**

Explanation:

The FlashArray//XR4 utilizes onboard 100GbE RoCE (RDMA over Converged Ethernet) ports for connecting to the first loop of DirectFlash Shelves, removing the need for dedicated PCIe add-in cards for the base configuration. The port mapping for these onboard backend ports differs from previous generations.

On the //XR4 controller chassis, the specific Ethernet interfaces designated for the first DirectFlash Shelf loop are typically the high-numbered onboard ports. In this specific exam context and hardware revision, ETH 18 and ETH 19 are identified as the correct primary backend connectivity ports .

Implementation Engineers must connect the QSFP28 cables from the "uplink" ports on the first shelf (IOM0 and IOM1) to ETH18 and ETH19 on the controllers (CT0 and CT1) respectively. Using incorrect ports (like ETH0/1, which are management) would result in the shelf not being detected by the storage fabric.

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### NEW QUESTION # 144

After racking a new FlashArray with one data pack, how should DirectFlash modules be installed?

- A. Starting in bay 19, right to left.
- B. Starting in bay 0, left to right.
- C. Starting in bay 10, left to right.

**Answer: B**

Explanation:

Proper airflow and thermal management are critical for the reliability of high-density storage arrays.

FlashArray chassis are designed with specific airflow baffles and cooling zones that rely on the drive bays being populated in a specific order.

When installing a new FlashArray with a single data pack (typically 10 drives), the Implementation Engineer must install the DirectFlash Modules starting in bay 0, filling from left to right .

\* Bay 0 is typically the leftmost slot (when facing the front of the array).

\* Filling slots 0-9 ensures that the first "cooling zone" is properly pressurized, forcing air through the populated modules and the chassis midplane correctly.

\* Leaving gaps (e.g., installing in slots 10-19 while 0-9 are empty) can disrupt the airflow path, potentially leading to hotspots or inefficient cooling for the controllers behind the backplane.

\* Additionally, the software enumeration of drives often expects contiguous population starting from the lowest index for logical clarity, though cooling is the primary physical constraint.

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### NEW QUESTION # 145

What command should the Implementation Engineer run to view NVRAM install and update status?

- A. purefw list
- B. purearray list
- C. puredrive list
- D. purehw list --all

**Answer: C**

Explanation:

Within the Purity//FA operating system architecture, dedicated NVRAM modules (used heavily in standard non-DFMD arrays to provide non-volatile write caching) are fundamentally treated as specialized drives by the software layer. They are physically installed

into specific central chassis bays labeled NVB0, NVB1, NVB2, and NVB3.

Because they are classified as drive components, the primary and most direct command an Implementation Engineer should use to verify their physical installation, health, capacity, and update status is `puredrive list`.

When this command is executed via the CLI, it generates a comprehensive table detailing every DirectFlash Module (DFM) and NVRAM module currently seated in the chassis.

The output explicitly shows the slot location (e.g., CH0.NVB0), the component's operational status (healthy, empty, evacuating, or updating), and its specific firmware version. While the `purehw list` command is excellent for viewing broader chassis components (like fans, temperature sensors, and controllers), `puredrive list` is the purpose-built command required to monitor the precise synchronization and firmware update phases of the NVRAM modules, especially crucial during a non-disruptive upgrade (NDU) when ensuring cache mirror integrity is paramount.

#### NEW QUESTION # 146

Refer to the following output:

Ping successful with CCM

What does this indicate?

- A. Controller has successfully connected to the Fusion Fleet Coordinator
- B. Cross-controller link has successfully connected between controllers
- C. Controller has successfully connected to pure1

**Answer: C**

Explanation:

The output "Ping successful with CCM" is a specific success message returned by the `pure support test` or `pure array test connectivity` checks. CCM stands for Cloud Connection Manager, which is the internal service or endpoint responsible for mediating the secure connection between the local FlashArray and the Pure1 cloud management platform.

When an Implementation Engineer sees this message, it confirms that the array can successfully resolve and reach the Pure1 infrastructure over the internet (specifically the `pure1.purestorage.com` or associated regional endpoints). This validates that: DNS is functioning correctly (resolving the CCM hostname).

Firewall rules are permitting outbound HTTPS (port 443) traffic.

The array's management interface is routing correctly.

This connection is vital for "Phone Home" logs, Remote Assist sessions, and fleet management via the Pure1 mobile app or dashboard. It is distinct from the Fusion Fleet Coordinator (which manages fleet logic) and the cross-controller interconnect (which is internal hardware communication).

#### NEW QUESTION # 147

The Pure Engagement Request (PER) specifies that iSCSI ports ETH2 and ETH3 should be set to 10 Gb/s. After configuring the ports and connecting them to the SAN, the Implementation Engineer observes that ETH2/3 are not negotiating and display 0 b/s. The SAN is operating at 40 Gb/s, with support for up to 100 Gb/s. What should the Implementation Engineer do to resolve this issue and complete the install?

- A. Force negotiate the switch iSCSI ports to 40 Gb/s.
- B. Replace the transceivers with the appropriate type.
- C. Force negotiate the array iSCSI ports to 40 Gb/s.

**Answer: B**

Explanation:

This scenario describes a physical layer mismatch between the FlashArray optics and the customer's switch infrastructure.

The PER (planning document) specified 10 Gb/s, so the Implementation Engineer likely installed 10 Gb SFP+ transceivers into the array.

The SAN Switch is operating at 40 Gb/s (likely using QSFP+ ports).

You cannot simply "force negotiate" a 10Gb SFP+ optic to run at 40Gb/s, nor can you plug a 10Gb SFP+ directly into a 40Gb QSFP+ port without specific breakout cables or QSA adapters that match the signaling. The physical transceivers themselves are incompatible with the link speed required by the switch.

To resolve this, the Implementation Engineer must replace the transceivers with the appropriate type.

If the switch is 40Gb native, the array needs 40Gb (QSFP+) optics (if supported on that slot).

Alternatively, if the customer intends to use 10Gb, they must provide 10Gb ports on their switch side.

Given the prompt implies the SAN is 40Gb, the 10Gb optics in the array are the incorrect hardware for that link.

## NEW QUESTION # 148

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